WHAT IS CLAIMED IS:

1. A method for controlling a semiconductor memory, the method comprising the steps of:

5   changing the semiconductor memory from burst mode, through power-down mode, to standby mode of non-burst mode in the case of setting a mode register for setting an operation mode in the burst mode;

changing the semiconductor memory from the standby

10   mode of the non-burst mode to mode register set mode in the case of commands being input in predetermined sequence in the standby mode of the non-burst mode; and

setting the mode register according to input from outside.

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2. The method for controlling a semiconductor memory according to claim 1, wherein the mode register includes a bit for prohibiting resetting, further wherein the contents of the mode register are not reset in the

20   power-down mode if the bit has been set.

3. The method for controlling a semiconductor memory according to claim 1, wherein the predetermined sequence includes a set of six commands of one read

25   command combined with the most significant bit of an address, four write commands each combined with the most significant bit of the address, and the one read command

combined with the address indicative of the operation mode.

4. A semiconductor memory comprising:

a mode setting control circuit with a mode register
to set an operation mode for setting the mode register in
the case of commands being input in predetermined sequence
in standby mode of non-burst mode; and

a power-down control circuit for changing the
semiconductor memory from standby mode of burst mode,
through power-down mode, to the standby mode of the non-
burst mode.

5. The semiconductor memory according to claim 4,
wherein the mode register includes a bit for prohibiting
resetting, further wherein the contents of the mode
register are not reset in the power-down mode if the bit
has been set.

6. The semiconductor memory according to claim 4,
wherein the predetermined sequence includes a set of six
commands of one read command combined with the most
significant bit of an address, four write commands each
combined with the most significant bit of the address, and
the one read command combined with the address indicative
of the operation mode.